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Annual Letter Report

on

tinued Development and Characterization of Doped Layers,
tacts and Associated Electronic Devices in Silicon Carbide

Supported by ONR Under Contract N00014-88-K-0341

For the Period April 1, 1988 – September 30, 1988

School of Engineering

North Carolina State University

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UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION Unclassified	1b. RESTRICTIVE MARKINGS N/A
2a. SECURITY CLASSIFICATION AUTHORITY N/A	3. DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; distribution unlimited
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A	
4. PERFORMING ORGANIZATION REPORT NUMBER(S) NCS-MAT/E-001	5. MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION North Carolina State Univ. 6b. OFFICE SYMBOL (If applicable)	7a. NAME OF MONITORING ORGANIZATION ONR - Code 1212
6c. ADDRESS (City, State, and ZIP Code) Dept. Materials Science & Engineering Box 7907, Raleigh, NC 27695-7907	7b. ADDRESS (City, State, and ZIP Code) Arlington, VA 22217
8a. NAME OF FUNDING/SPONSORING ORGANIZATION ONR 8b. OFFICE SYMBOL (If applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER N00014-88-K-0341
8c. ADDRESS (City, State, and ZIP Code) Applied Research Division Code 1212 800 N. Quincy St., Arlington, VA 22217-5000	10. SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO. / PROJECT NO. / TASK NO. / WORK UNIT ACCESSION NO.

11. TITLE (Include Security Classification)
Continued Development and Characterization of Doped Layers, Contacts and Associated Electronic Devices in Silicon Carbide

12. PERSONAL AUTHOR(S)
R. F. Davis

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
Annual Letter	FROM 4/1/88 TO 9/30/88	10/31/88	30

16. SUPPLEMENTARY NOTATION

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

The primary thrust of research of this period has been to deposit and characterize the contact materials of $TaSi_2$ and Al on n- and p-type material, respectively. Auger electron spectroscopy detected some oxygen throughout the thickness of these films. Current voltage characteristics were non-linear and highly resistive due to oxygen contamination in the films. A new ultra-high vacuum deposition chamber is being constructed to deposit pure contacts. Rectifying contacts of Au, Pt, and $PtSi_x$ were also studied. Pt surpassed Au in its rectifying properties. Ion implantation into alpha and beta SiC at room temperature and 550°C were also conducted. A new capacitance voltage system was purchased and commissioned.

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT ☐ UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT ☐ DTIC USERS	21. ABSTRACT SECURITY CLASSIFICATION Unclassified
22a. NAME OF RESPONSIBLE INDIVIDUAL Robert F. Davis	22b. TELEPHONE (Include Area Code) (919) 737-3272 22c. OFFICE SYMBOL

DD FORM 1473, 84 MAR — 83 APR edition may be used until exhausted. All other editions are obsolete.

SECURITY CLASSIFICATION OF THIS PAGE
UNCLASSIFIED

154-203

1. Introduction

Silicon carbide is the only compound species that exists in the solid state in the Si-C system, but it can occur in many polytype structures. The lone cubic polytype crystallizes in the zinc blende structure and is denoted as β-SiC. The ~170 known additional hexagonal and rhombohedral polytypes are collectively referred to as α-SiC. The electron Hall mobility of high-purity undoped β-SiC has been postulated from theoretical calculations to be greater than that of the α forms over the temperature range of 300–1000K because of the smaller amount of phonon scattering in the cubic material. Although this result has served as one catalyst for the current international interest in β-SiC, this material also possesses a unique combination of additional properties including a high melting point (3103K at 30 atm), high thermal conductivity (3.9 W/cm•deg), wide band gap (2.2 eV at 300 K) and high breakdown electric field (2.5×10^6 V/cm). As such, β-SiC has been theoretically shown to be superior to Si, GaAs or InP using either Johnson's or Keyes' figure of merit for high-frequency, high-speed and high-power transistor applications.

The high thermal conductivity and breakdown field also indicate that the integration of devices made from β-SiC can be achieved with high densities. Two additional reasons for the renewed interest in β-SiC are the significant advances in the growth of monocrystalline thin films of this material by chemical vapor deposition (CVD) and the ability to dope this material with n- and p-type dopants growth or via ion implantation. As a result, devices from this material have now become a reality.

In this reporting period, we have concentrated on the development of more suitable ohmic and rectifying contacts to β- and α-SiC. Experiments regarding the search for an introduction of electrically active impurities by ion implantation have also been conducted. Both of these studies are continuing. The knowledge gained from these studies will be used in the fabrication of new devices now in the design stage. The experimental directions and results of this research are briefly described below.

2. Ohmic Contacts to Beta Silicon Carbide

The primary thrust of research of this period has been to characterize the currently used contact materials, $TaSi_2$ and Al, on n-type and p-type material, respectively. The metallization was accomplished by RF sputtering. Most samples had Shockley patterns delineated by photolithography for measurement of contact resistance by the transfer length (TLM) method.

Rutherford backscattering spectrometry of films sputtered from a $TaSi_2$ target revealed that the film stoichiometry matched that of the target. This technique detected no differences between as-deposited films and films annealed at 1000°C for 300 s. Auger electron spectroscopy detected some oxygen throughout the thickness of these films. Depth profiles show strong indication of SiO_x on the surface and at the $TaSi_2$/SiC interface. Thin film analysis of the Al contacts has not yet been conducted.

Contact resistance measurements were conducted using the transfer length method (also known as the transmission line model, TLM). The test structure is a linear, six terminal Shockley pattern consisting of six rectangular (200 × 80 micron) pads separated by 50, 30, 20, 10, and 5 microns. Current-voltage characteristics were non-linear and highly resistive. This is probably due to oxygen contamination in the films noted above. Linear current-voltage characteristics are needed for this technique to work.

The next step in this program will be obtaining oxygen free, low resistance films so that relevant data can be obtained. The problem may be caused by thin native oxide films and/or leaks in the chamber of the sputtering system. Once the oxygen is eliminated, data on interface reactions and contact resistance will be obtainable. A new ultrahigh vacuum electron beam deposition chamber is being constructed in order to deposit oxygen-free metallic and silicide contacts on α- and β-SiC.

In addition to the characterization techniques noted above, cross-sectional TEM, and modified and cylindrical TLM techniques will be used to characterize the contacts. Once the established materials have been examined, other metals (such as NI, W, Ta, and Ti) will be studied. The ultimate goal is to fabricate reliable and reproducible contacts, and measure their properties which will affect device design and performance.

3. Rectifying Contacts to Beta Silicon Carbide

Current-voltage characteristics of Au contact diodes formed on β-SiC films grown on both nominally (100) oriented and off-axis (100) silicon substrates have been investigated. These characteristics are dominated by deep-level states. The nominal (100) substrate has two deep-levels and in some cases also additional traps distributed exponentially in energy, whereas the off-axis material has only one deep trap. These Au contact diodes do not appear to be suitable as rectifying contacts for high-temperature devices, as a 400°C heat-treatment degrades diode characteristics considerably. However, valuable information about the electrical characteristics of grown films can be obtained from simple I-V measurement at room temperature. A manuscript regarding this research on Au contacts on SiC authored by Das *et al* and submitted for review and future publication is attached to this report as Appendix I.

Preliminary work conducted on Pt contact diodes indicate that these are in some ways superior to Au contact diodes. In particular, Pt diodes are not degraded as a result of bias stressing, although for –5 V to 5 V operation Pt diodes have a higher leakage current than Au diodes. Platinum silicide contacts are expected to perform better. However, experimental difficulties have so far prevented the fabrication of Pt silicide contacts.

4. Ion Implantation Into Beta Silicon Carbide

Implantation of Al ions in β-SiC is being conducted for the fabrication of junction-diodes with reproducible characteristics and also for the formation of a uniform p-type doped layer. The uniform p-doped layer, if successfully formed, should serve as a substrate for further growth of an n-type layer thereby permitting the fabrication of MESFETs. The uniform p-layer may also enable the fabrication of NMOSFETs.

5. Ion Implantation Into Alpha Silicon Carbide

Ion implantation studies in α-SiC have been initiated. Samples of sublimation grown bulk α-SiC were implanted at Oak Ridge National Laboratories with N and Al. Conditions of implantation are listed in Table 1. Rutherford Backscattering was performed in the channeling mode on all samples. As with β-SiC, implantation at elevated temperatures (550°C) produced much less damage than room temperature implantation. Analysis of the damage by TEM is underway at ORNL and characterization of carrier properties by C-V measurements is being conducted at NCSU. Initial problems with acquiring good ohmic contact to the α-SiC have been overcome.

Table 1

Sample	Species	Energy (KV)	Dose (cm^{-2})	Peak Concentration	Temperature (°C)
060288-1	N+	110	6.58×10^{14}	5×10^{19}	RT
060288-2	N+	110	6.58×10^{14}	5×10^{19}	550
060288-4	N+	55	6.58×10^{14}	5×10^{19}	550
060388-6	AL+	200	6.62×10^{15}	5×10^{20}	RT
060388-7	AL+	200	6.62×10^{15}	5×10^{20}	550
060388-8	AL+	110	6.62×10^{15}	5×10^{20}	550

6. Capacitance-Voltage Measurement System

An electronic system to measure capacitance has been purchased and commissioned. This system consists of a Keithley 590 high frequency capacitance meter, 595 quasistatic capacitance meter, 230–1 voltage source, a switching unit to allow simultaneous measurements, and a Hewlett-Packard PC308 Vectra computer operating with Keithley software on an HP Basic language processor card. Production of test capacitors in β-SiC is underway.

APPENDIX 1

DEEP-LEVEL DOMINATED ELECTRICAL CHARACTERISTICS OF Au CONTACTS ON β-SiC

K. Das, H. S. Kong, J. B. Petit, J. W. Bumgarner and R. F. Davis
Department of Materials Science and Engineering
North Carolina State University, Box 7907
Raleigh, North Carolina 27695-7907

and

L.G. Matus

National Aeronautics and Space Administration
Lewis Research Center, Cleveland, Ohio 44135

Abstract

Current-voltage characteristics of Au contacts formed on β-SiC films grown heteroepitaxially on both nominally (100) oriented and off-axis (100) silicon substrates have been investigated. These contact diodes are rectifying and particularly in off-axis silicon substrates very low reverse leakage currents are observed. The diode ideality factor is between 1.3 and 2.0 in all cases except in nominal (100) silicon substrates where it is greater than two. Logarithmic plots of the I-V characteristics in the forward direction indicate space charge limited current conduction through the active volume of the diodes. The β-SiC films grown on nominally (100) oriented substrates show the presence of two deep levels located approximately between 0.26 eV and 0.38 eV below the conduction band edge. In some films on nominal (100) substrates, the I-V characteristics are also influenced by some additional traps which are exponentially distributed in energy with a maximum occurring at the conduction band edge.

In contrast the films deposited on off-axis substrates have only one deep level located approximately below 0.49 eV for the 2° off (100) substrates and at 0.57 eV for the 4° off (100) substrates.

Previous microstructural analysis revealed that the nature and density of defects in the β-SiC heteroepitaxial films on both nominal and off-axis (100) silicon are similar except that the films on nominal (100) substrates have a high density of antiphase domain boundaries. Therefore, the presence of the shallower deep-level states observed in the β-SiC films grown on nominal (100) substrates is speculated to be due to the electrical activity of antiphase domain boundaries.

Introduction

Metal-semiconductor contacts commonly referred to as Schottky-barrier diodes have been investigated for many years for their scientific interest and technological importance[1]. These contacts, regardless of the mechanism involved in their operation are in most cases rectifying[2]. In most experimental structures the barrier height at the interface is not what is expected from work function differences. Complexities arise from the presence of interface states, interfacial insulator layers, barrier lowering, interface chemistry, and tunneling of carriers through a thin barrier[3,4]. Transport of carrier through the barrier is also complicated due to tunneling, recombination, diffusion and bulk semiconductor resistance effects. These transport factors are in addition to thermionic emission normally expected in a true Schottky type behavior characterized by an ideality factor of 1[3,4]. For any departure from the idealized description, values of n greater than 1 will be obtained. Current transport[5,6] as well as barrier capacitance[7,8] are also profoundly influenced by the presence of deep level states.

Although a great deal of understanding and insight have been developed regarding the nature of metal-semiconductor contacts, still not all experimentally observed features can be adequately interpreted. Nevertheless, technological achievements have been noteworthy. For example, near ideal reverse characteristics have been demonstrated and reduced charge storage and improved switching times have been obtained in Schottky clamped transistors[1]. Advanced devices fabricated in GaAs mostly rely on Schottky barrier gates for their operation. Adjustment of the barrier height to a required value is also possible by introducing an ion-implantation step[9].

Gold contacts on SiC have been studied by a relatively small number of workers[10-13]. A near-ideal Schottky barrier with n of 1.02 was observed by Wu and Campbell[10] in bulk α-SiC. A value of n of 1.45 was reported by Hagen[11] on similar materials. In heteroepitaxial β-SiC films deposited on Si substrates, Ioannou et al. observed that the forward current-voltage (I-V) characteristics were exponential over six orders of magnitude and reported an ideality factor of 1.5[12]. However, in their study of Au contacts on β-SiC, Yoshida *et al.*[13] did not observe such an exponential behavior and their ideality factor ranged between 1.4 and 2.0. A linear regime, in the logarithmic plots of the forward characteristics of these devices, was indicative of space charge limited current (SCLC) conduction[13]. In the present study, values of n between 1.3 and 3.5 were observed in devices fabricated in a number of different β-SiC films. The deviation of the ideality factor from 1 in these crystals and the detailed structure of forward characteristics appear to be due to SCLC conduction mechanism in SiC. Observation of SCLC in both α and β–SiC has been reported previously[14-17].

Space charge limited current flow in insulators and wide band gap semiconductors have been considered in detail by Lampert and Mark[18]. True SCLC is characterized by a square-law dependence on voltage. Initially ohmic behavior is observed if thermally generated free carriers are present. If deep traps located below the equilibrium Fermi level are present, ohmic behavior will be observed until all the trap levels are filled. At this point a sharp rise followed by square law behavior will be observed in the I-V curve. For traps above the Fermi level, termed shallow-traps by Lampert and Mark, a trapped square law behavior is also observed at a lower bias. When these latter traps are filled, current rises rapidly to true SCLC square law regime. One is likely to obtain an n value much greater than 1, if the sharp rise in current is interpreted as an exponential function given by

$$I \propto e^{\frac{qV}{nkT}} .$$

Traps distributed in energy may occur due to a high density of defects.[19-22]. Current voltage characteristics, in the presence of traps distributed in energy, may not exhibit all the features of SCLC discussed above. In particular, the sharply rising regime in current may not be evident, although a power-law of greater than one is likely to be observed.

A detailed analysis of the aforementioned fine-structure in the I-V characteristics can reveal information pertaining to the deep-states as well as their effect in a realistic device operation situation, since the metal/semiconductor contact forms a basic component of a number of solid state devices.

A previous study[17], in the authors' laboratory, of ion-implanted p-n junction diodes in β-SiC revealed the presence of two trapping levels in the lower third of the band-gap. These were located 0.22eV and 0.55 eV above the valence band edge with approximate densities of 2×10^{18} cm^{-3} and 2×10^{16} cm^{-3} respectively. The former was believed to be ionized Al centers (in the case of an Al-implanted sample) and the latter a compensating acceptor level. These observations were compatible with the deep level transient spectroscopy (DLTS) data on β-SiC reported by Nagesh *et al.*[23] who observed no deep trapping levels in the upper third of the band gap. However, Zhou *et al.*[24] reported the presence of two trap levels, 0.34 and 0.68eV below the conduction band as determined by DLTS on β-SiC. The deeper trap appeared to be formed as a result of high temperature thermal oxidation. The presence of these traps was not reflected in the I-V characteristics of our implanted diodes.

A study of Au β-SiC contacts on both nominal and off-axis (100) silicon substrates has been conducted and is reported here. A high density of antiphase domain boundaries (APB's), in the films on nominal (100) silicon substrates appear to contribute to two deep levels below the conduction band and also in some cases to additional traps exponentially distributed in energy with a maximum at the conduction band edge. In contrast, in films on off-axis substrates, only one level is observed. These deep-level states affecting the I-V characteristics of these Au β-SiC contact diodes appear to be located in the upper third of the band gap, similar to those reported by Zhou *et al*[24]. The present study on Au β-SiC contact diodes and the previous study on implanted junction diodes[17] clearly indicate that I-V characteristics of the majority and minority carrier devices are affected by different sets of deep level states. This behavior is not entirely unexpected considering the quasi-Fermi levels in majority and minority carrier devices, in the presence of injected carriers, are likely to be very different. Consequently, the occupation probabilities of the

Lanyon[20] has emphasized that SCLC I-V characteristics can only give information about the distribution of states in the limited energy region through which the quasi-Fermi level passes.

Experimental

β-SiC films were epitaxially grown on nominal and on off-axis silicon substrates by chemical vapor deposition (CVD). At the NCSU laboratory a cold-wall vertical, barrel-type rf-heated system was employed for the deposition (see ref. 25 for system details). Silane (SiH_4) and ethylene (C_2H_4) carried in hydrogen were employed as the Si and C sources, respectively. Flow rates of the H_2, SiH_4 and C_2H_4 were 3000 sccm, 2 sccm and 1 sccm, respectively. The growth technique used to produce β-SiC films was the two-step method, which included chemical conversion of the Si surface followed by CVD (see ref. 26 for detailed growth procedures). The growth temperature was approximately 1360°C and the pressure was 1 atm. The β-SiC films grown at the NASA Lewis Research Center were produced in asimilar manner. In the NASA lewis process, a conventional cold-wall horizontal CVD reactor was utilized. process , silane and propane (C_3H_8) carried in hydrogen, provide the necessary Si and C sources for β-SiC growth (see ref. 27 for complete system and growth process description).

These layers were not doped intentionally; however, a net electron concentration of $\sim 1 \times 10^{17}$ cm^{-3} were obtained in these films. The grown films were polished using 0.1μm diamond paste for 48 hours. A layer approximately 1.2 μm in thickness was removed by this process. The wax residue from the polishing process was cleaned in hot concentrated H_2SO_4. A final cleaning was carried out using a 1:1 mixture of H_2SO_4 and H_2O_2 followed by a 2min dip in buffered oxide etch. In order to remove the damage caused by the polishing process, an oxide layer of ~1000Å in thickness was grown in a dry oxygen ambient at a temperature of 1200°C. The oxide layer was etched and a layer of gold, ~2000Å in thickness, was thermally evaporated on the samples to form devices were separated from the field region by a 100 μm wide annular ring. The structure of these diodes were similar to those reported by Ioannou *et al.*[12]. A measurement of I-V characteristics between the active device and the field region was conducted out using an HP 4145A semiconductor parameter analyzer. Current-voltage measurements as a function of temperature between 25°C - 150°C were obtained for the diodes on NCSU 870626/1, in order to establish whether thermionic emission was the prevailing conduction mechanism. This procedure was also expected to yield the barrier height and the modified Richardson's constant[1]. However, at elevated temperatures of 50°C and above, ohmic conduction at low forward biases was observed indicating the non-thermionic character of the contact diodes. Room temperature measurements were also carried out on these diodes following a 30 minute anneal at 400°C, in order to establish any thermal degradation of the contacts. Capacitance measurements at 1 MHz were carried out using a Keithley 590 CV analyzer.

Results and Discussions

The current-voltage characteristics of the metal-semiconductor contact diodes fabricated in β-SiC on nominal (100) and off-axis (100) silicon substrates are shown in Fig. 1. The linear plots in Fig. 1(a) show asymmetric behavior, *i.e.*, rectification. The observed reverse currents in these diodes, values of the ideality factor, and also deep-level parameters are given in Table I. The diodes in films deposited on the nominally (100) oriented substrates have higher reverse currents. The semi-logarithmic plots of the measured data are shown in Fig. 1(b). Values of n greater than 2 indicate that a mechanism other than thermionic emission was dominating current transport in these devices. Indeed, an ohmic slope at low biases (0.01V-0.1V) as seen in the logarithmic plots of Fig. 1(c) is a clear indication of non-thermionic behavior. Features in the I-V characteristics strongly indicating SCLC conduction in the presence of deep-level states become evident at higher later in this section.

In the nominal (100) plot shown in Fig. 1(c), the transition from an ohmic regime to a sharply rising current regime is an indication of the presence of deep traps. Normally a sharp rise to a true SCLC level is obtained when all the deep traps are filled, (see Fig.1 (a) and plot 1 of Fig. 2), the voltage at which this occurs is designated by V_{TFL}, where TFL denotes trap-filled-limit. In the active region of the diode, the hole occupancy of the traps or the concentration of traps not occupied by electrons, p_{to}, is obtained from the estimated value of V_{TFL} given by

$$V_{TFL} \sim \frac{q p_{to} L^2}{\varepsilon \varepsilon_0} , \qquad (1)$$

where

L = the thickness of the active region

q = the electronic change

ε = the dielectric constant, and

ε_0 = the permittivity of free space.

The effective carrier concentration in the active region, n_0, is given by the approximate relation[18]:

$$\frac{J(2V_{TFL})}{J(V_{TFL})} \sim \frac{p_{to}}{n_o} , \qquad (2)$$

where J is the current density. In the diodes studied, values of n_0 range between 10^9 cm^{-3} and 10^{13} cm^{-3}, whereas the bulk carrier concentration in the films is of the order of 10^{17} cm^{-3}. The low effective carrier concentrations in the active volume of the diodes are probably an indication of level. As such, p_{to} is the concentration of the unoccupied state located approximately at the estimated Fermi level. (Table 1).

In the diodes fabricated in films on off-axis substrates, the current at low forward biases is independent of bias as shown in Fig. 1(c). The voltage at which the sharp rise in current occurs is taken as V_{TFL}. A given choice of V_{TFL} determines the value of p_{to}, however, the position of the deep-level is primarily determined by the slope of the sharply rising regime in current.

In these diodes in the off-axis material, a single discrete deep level is normally observed. In the 2° off-axis material, NASA 816/4, the deep level is located at 0.49 eV and in the 4° off-axis, NCSU 870626/1, 0.57 eV below the conduction band with respective concentrations of unoccupied states of 5.0×10^{15} cm^{-3} and 5.2×10^{15} cm^{-3}.

In a number of diodes in films on the off-axis substrates, a change in slope is observed at the end of sharply rising current regime, as shown in plot 2 of Fig. 2. This change in slope is interpreted to be due to filling of two sets closely located deep level traps. In NASA 721/6 these traps are 0.33 eV and 0.4 eV below the conduction band with concentration of unoccupied states of 1.2×10^{15} cm^{-3} and 2.5×10^{15} cm^{-3} respectively. A small number of diodes in 8707/5 also showed an ohmic regime at room temperature, as shown in plot 1 of Fig. 2. Nonuniformities in defect distribution and carrier concentrations are suspected to be the origin of these observed features. At low forward biases, diodes fabricated in films on nominal (100) substrates conduct a much higher current than those on off-axis substrates. In a number of cases, an ohmic regime is initially observed (NASA 816/2) and the rise in current following V_{TFL} is not very sharp. In this case $I \propto V^3$. This is considered to be an indication of smearing of the states due to electrical activity of crystallographic defects in the material[20]. However, for the simple analysis using eqns. (1) and (2) only one discrete level is considered. In NASA 816/2 this level is located at 0.26 eV below the conduction band with a concentration of 6.6×10^{15} cm^{-3} of unoccupied states, whereas in NCSU 870130 a similar level is located 0.32 eV below the conduction band with 3.8×10^{15} cm^{-3}

870130 with concentration of unoccupied states as 3.8×10^{15} cm^{-3} and 3.0×10^{15} cm^{-3}, respectively. In NCSU 870130, the current initially is proportional to $V^{1.6}$. This super-linear behavior can be conveniently described by an exponential distribution of traps given by[19,20]

$$N(E) \sim N_0 e^{E/\Delta} ,$$

where

N_0	=	density of trap states at the conduction band edge,
$N(E)$	=	density of trap states at an energy E below the conduction band, and
Δ	=	a thermal energy parameter characterizing the trap distribution.

The SCLC is given by

$$= Aq\,\mu\, N_c \left(\frac{\varepsilon\varepsilon_0}{qN_0\Delta}\right)^{\Delta/kT} \left(\frac{V^{\Delta/kT\,+\,1}}{L^{2\Delta/kT\,+\,1}}\right) , \qquad (3)$$

where $\Delta/kT+1$ is equal to m, the observed exponent of the experimental I-V curve, i.e. $I \propto V^m$. A characteristic temperature, such that $\Delta = kT_t$, has been defined by Rose [19]. However, the physical significance of temperature T_t is not clear[18]. A value of N_0 of 3.1×10^{16} cm^{-3} eV^{-1} is obtained with eqn. (3) using the following

$$\Delta = (m-1)kT = (1.6-1)kT = 0.6kT$$

$$= 0.0156 eV$$

$$I = 1 \times 10^{-9} A$$

$$V = 0.054 V$$

$$A = 7.8 \times 10^{-5}\ cm^2$$

$$\mu = 200\ \mathrm{cm^2/V\ sec}, \text{ and}$$

$$N_c = 1.5\times10^{19}\ \mathrm{cm^{-3}}$$

The slope of the SCLC part of the I-V characteristics following trap-filling varies from 1.5 to 1.9. It is probable that a resistive component or high-level injection effects will have degraded the ideal slope of 2.

A previous microstructural study established the presence of antiphase domain boundaries (APB's) in the heteroepitaxial β-SiC films deposited on nominal (100) Si substrates. These faceted boundaries and also contain a high density of dislocations. These defects are mostly eliminated by depositing β-SiC on off-axis (100) oriented Si substrates[26-28]. The density of defects other than APB's, namely stacking faults and microtwins, is comparable in heteroepitaxial films grown on both nominal and off-axis substrates. The high density of deep level states distributed in energy below the conduction band is, therefore, attributed to the electrical activity of the APB related defects.

Logarithmic plots of the reverse characteristics are shown in Fig. 3. In all cases except the devices on the off axis substrate at low reverse voltages, an ohmic regime is observed. Then a rapid rise in current occurs indicating either a localized edge breakdown or a rapid rise towards SCLC. These diodes show a very low leakage current too low to be measured using the present equipment which cannot measure currents lower than 1×10^{-10}A. A rapid rise in reverse current in the diode is obtained at a bias of ~-5V. The zero bias capacitance has been used to determine the effective device thickness for the calculation of deep-level parameters. Plots of $1/C^2$ as a function of voltage between 0 and -4V in most cases do not yield a straight line. However these plots appear approximately linear over a smaller range in voltage between 0 and -2V. This deviation is not entirely unexpected considering the presence of a high density of deep-level states in the material. Moreover, a variation in carrier concentration with depth can also be a contributing factor.

From the logarithmic plot of the forward characteristic it is clear that this heat treatment introduces deep-states, not present initially. A square-law regime preceding the sharp-rise indicates that the heat-treatment generated states are located above the quasi-Fermi level. The reverse leakage current increases by about two orders of magnitude probably through participation of the same deep states observed in the forward characteristic. This degradation is probably due to outdiffusion of Si from SiC matrix into the Au films[12]. The new deep-level states appear to be related to Si vacancies in the matrix.

Conclusions

Gold on heteroepitaxial β-SiC films deposited both on nominal (100) and off-axis (100) silicon form rectifying contact diodes. Very low reverse leakage currents are observed in diodes fabricated in films grown on off-axis silicon substrates. Although-the I-V and C-V characteristics indicate the presence of a barrier, the I-V characteristics are dominated by bulk effects rather than by thermionic emission over the barrier.

Logarithmic plots of the I-V characteristics in the forward direction indicate space charge limited current conduction through the active volume of the devices. The β-SiC films grown on nominally (100) oriented substrates show the presence of two deep levels located approximately between 0.26 eV and 0.38 eV below the conduction band edge. In some films on nominal (100) substrates, the I-V characteristics are also influenced by some additional traps which are exponentially distributed in energy with a maximum occurring at the conduction band edge.

In contrast β-SiC films deposited on off-axis substrates have only one deep level located approximately 0.49 eV below the conduction band edge for the 2° off (100) substrates and 0.57 eV for the 4° off (100) substrates. The shallower distributed deep states in the β-SiC on nominal (100) silicon substrates are attributed to the presence of antiphase domain boundaries in these films. A heat treatment at 400°C for 30 minutes considerably degrade the device characteristics. This heat treatment introduces extra deep-states not initially present in the material. Consequently, reverse leakage current increases by almost two orders of magnitude. Thus, Au contact diodes on β-SiC do not appear to be suitable as rectifying contacts for high-temperature device applications. However, valuable information about electrical characteristics of grown β-SiC epitaxial films can be obtained from simple I-V measurements on Au contact diodes.

Acknowledgements

The program was partially supported by NASA Lewis Research Center (Grant No. NAG 3-782) and the Office of Naval Research (Contract No. N00014-85-K-0182 P005).

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Table I. Reverse Current, Ideality Factor and Deep-Level Data Including the Position of Deep-Level States Below the Conduction Band-Edge, Concentration of Unoccupied Traps and V at the Trap-Filled Limit.

Substrate	I_r (A)	n	V_{TFL} (V)	Deep-level (E_c - eV)	Conc. p_{to} cm^{-3}
Nominal (100) Si NASA 816/2	1×10^{-3} (-5V)	3.5	0.125 0.215	0.26 0.38	6.6×10^{15} 3.8×10^{15}
Nominal (100) Si NCSU 870130	1×10^{-6} (-5V)	2.8	— 0.05 0.1	Exp., max at E_c 0.32 0.38	$N_0 = 3.1 \times 10^{16} cm^{-3} eV^{-1}$ 1.5×10^{15} 3.0×10^{15}
2° off-axis (100) Si NASA 816/4	1×10^{-7} (-10V)	1.45	0.48	0.49	5.0×10^{15}
2° off-axis (100) Si NASA 721/6	3.8×10^{-7}(-10V)	1.55/3.1	0.48 0.24	0.33 0.4	1.2×10^{15} 2.5×10^{15}
4° off-axis (100) Si NCSU 870626/1	6×10^{-8} (-10V)	1.3	0.5	0.57	5.2×10^{15}
4° off-axis (100) Si NCSU 870715	4.5×10^{-7} (-10V)	2.3	0.45	0.44	5.0×10^{15}
4° off-axis (100) Si NCSU 870626/1 following 400 °C heat treatment	1×10^{-6} (-10V)	1.23	— 0.2	Shallow-level 0.5	— 2×10^{15}

In deep-level calculations, thicknesses of the active regions of the diodes have been taken as 1.44×10^{-5} cm for the off-axis material and 2.23×10^{-5} cm for the nominal (100) material. These values have been determined from the average 0V bias capacitances. The dielectric constant of SiC is 9.3.

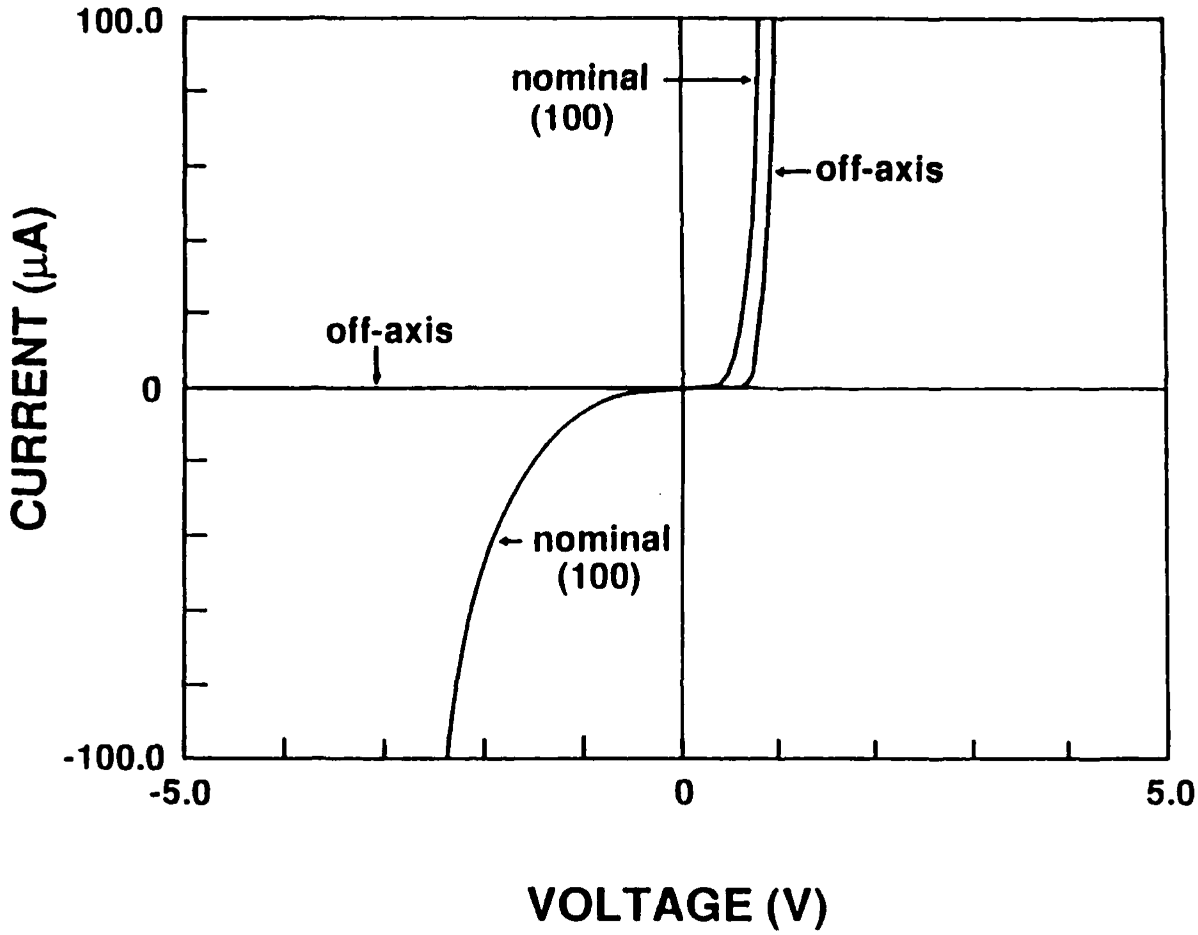

Fig. 1. (a). Linear plots of I-V characteristics for Au/β-SiC diodes on nominally (100) (NASA 816/2) oriented and off-axis (100) (NASA 816/6) silicon substrates.

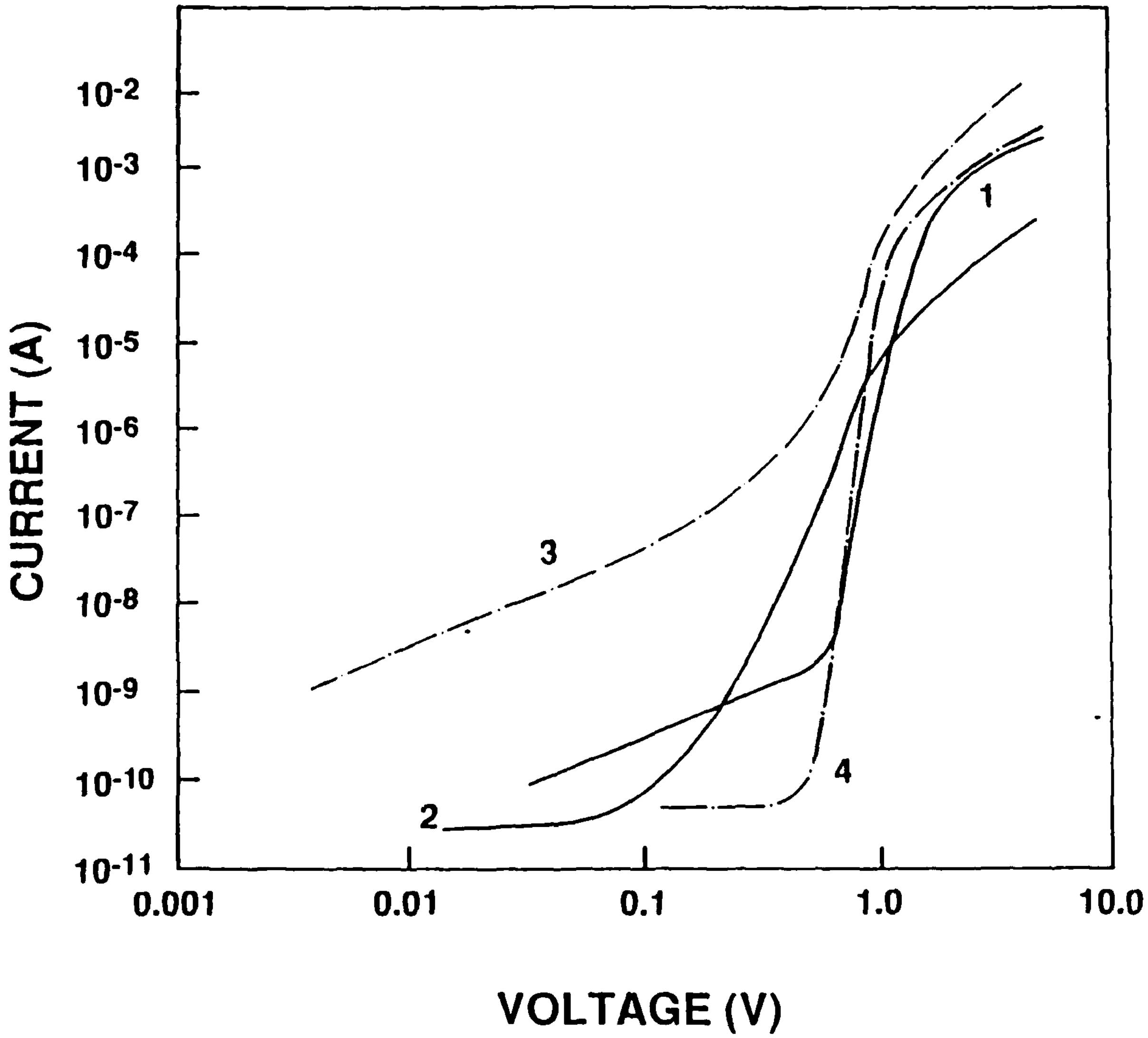

Fig. 2. Logarithmic plots of the forward characteristics of different diodes showing effects of localized nonuniformities in the carrier concentration and deep-level contributions. The dotted lines are considered to be representative characteristics. (1): 4° off-axis (100) Si (NCSU 870715), shows effect of higher carrier concentration than normal. (2): 2° off-axis (100) Si (NASA721/6), shows effects

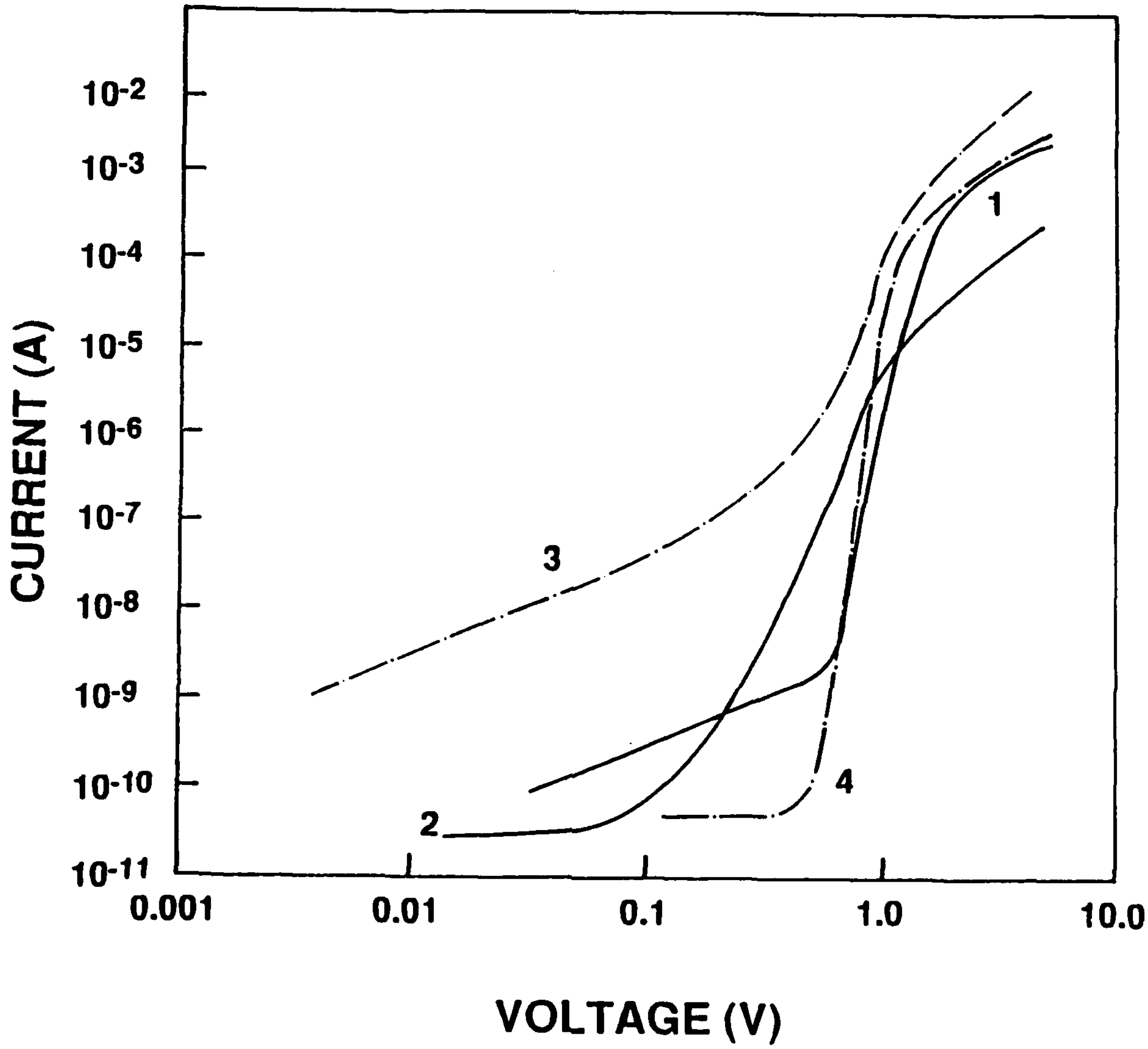

Fig. 2. Logarithmic plots of the forward characteristics of different diodes showing effects of localized nonuniformities in the carrier concentration and deep-level contributions. The dotted lines are considered to be representative characteristics. (1): 4° off-axis (100) Si (NCSU 870715), shows effect of higher carrier concentration than normal. (2): 2° off-axis (100) Si (NASA721/6), shows effects of two closely located deep levels. (3): Nominal (100) Si (NASA 816/2)

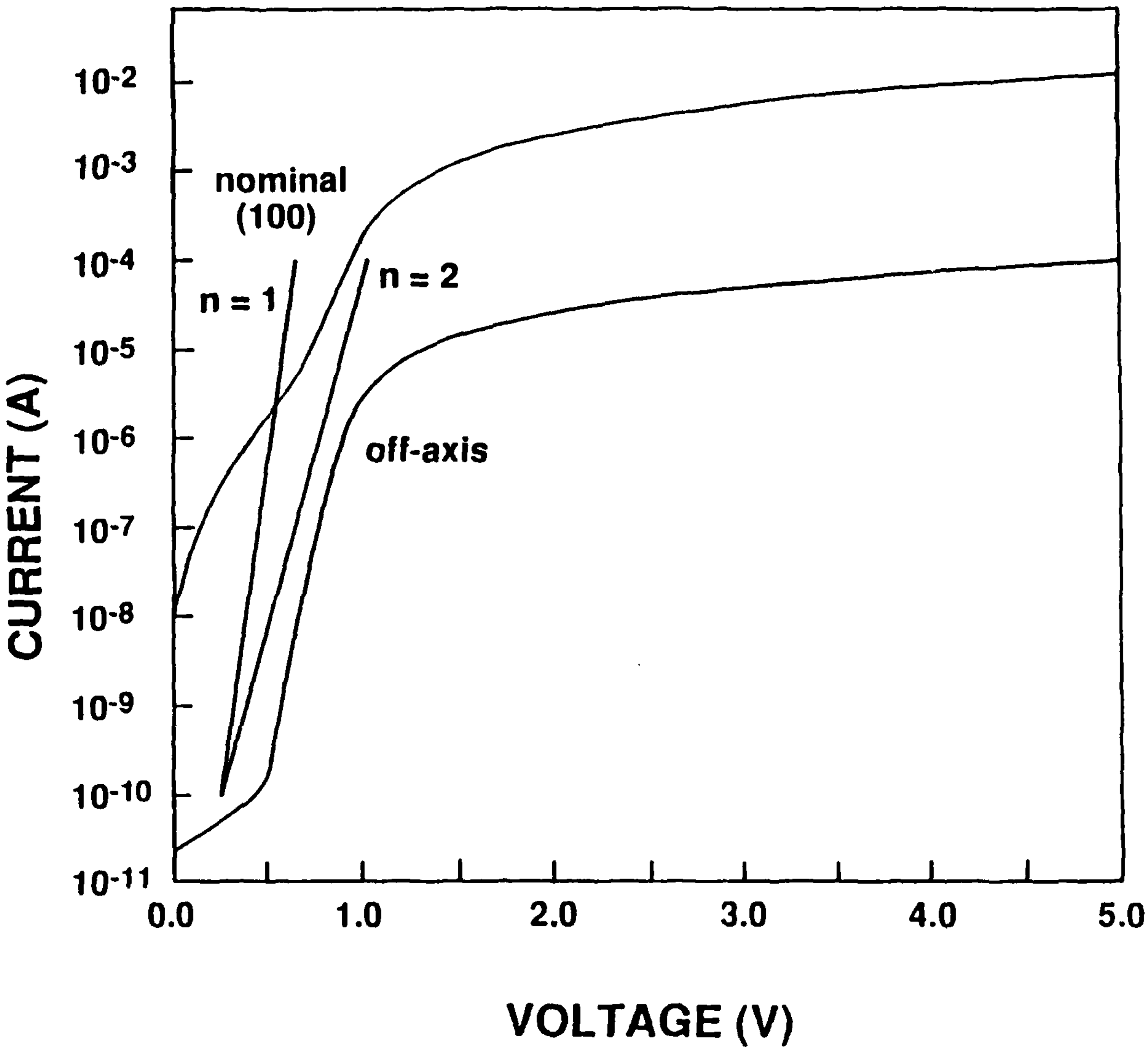

Fig. 1. (b). Semilogarithmic plots of the forward characteristics presented in Fig. 1. (a)

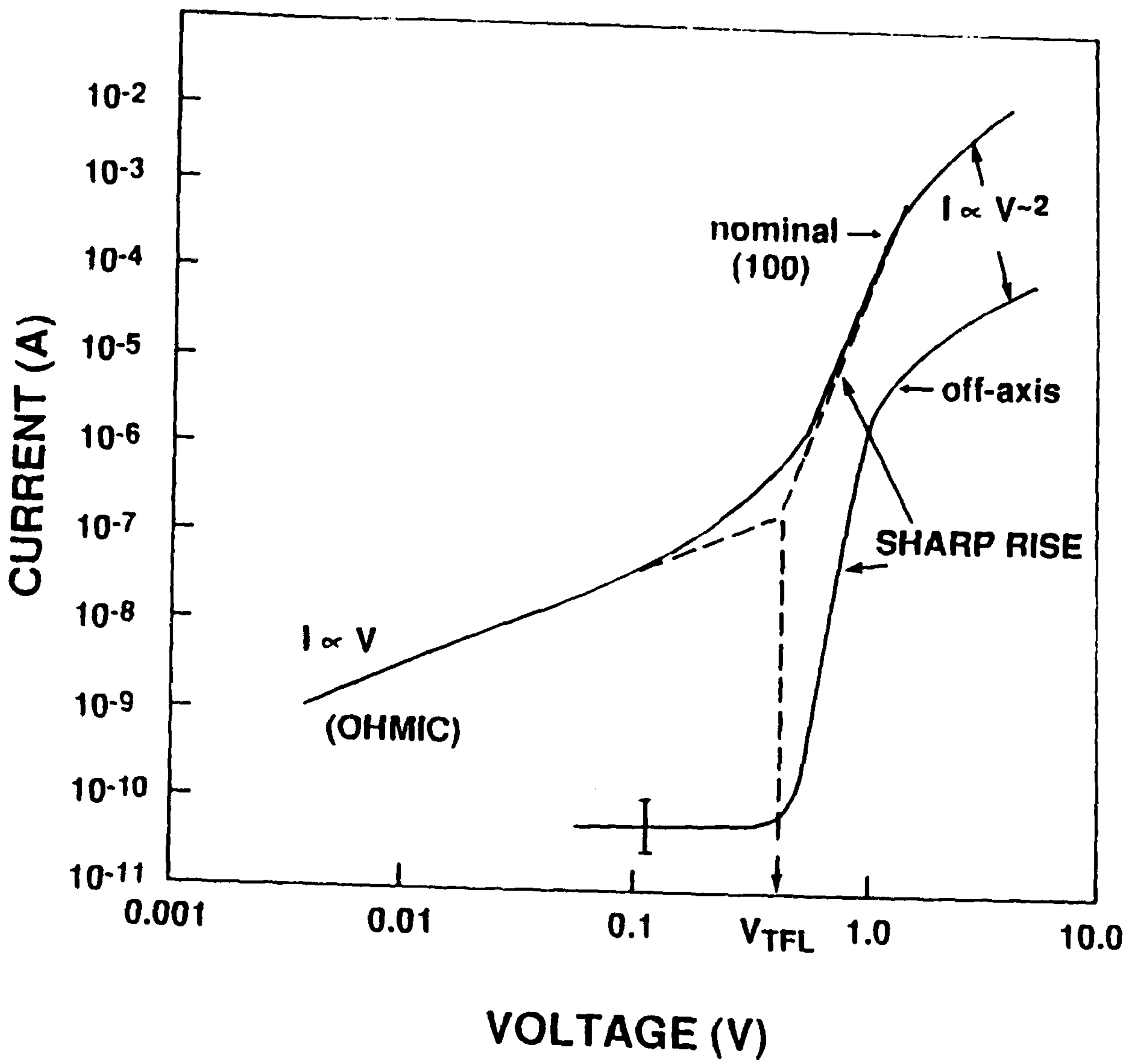

Fig. 1. (c). Logarithmic plots of the forward characteristics presented in Fig. 1. (a). Error bar represents maximum noise amplitude at low currents.

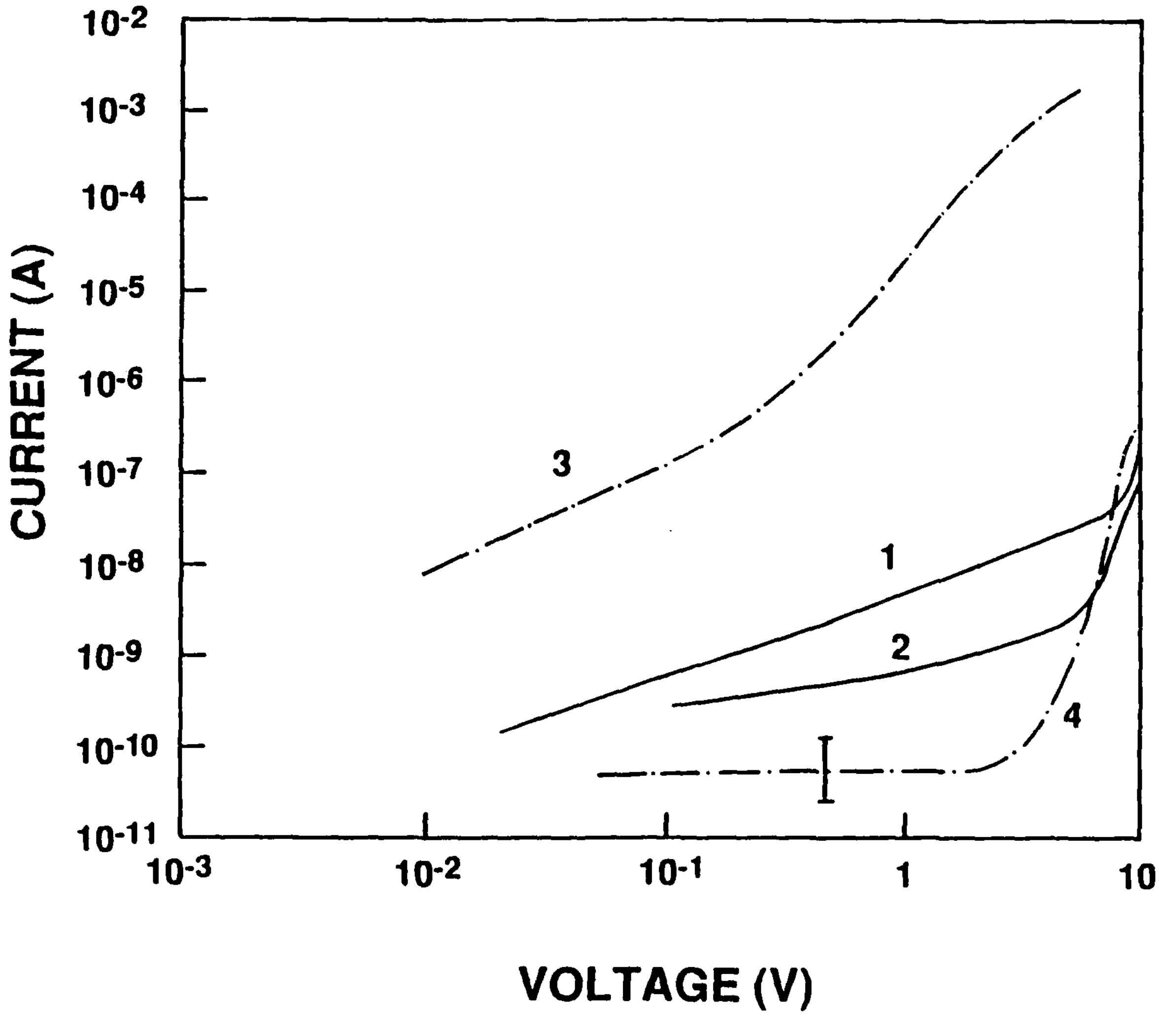

Fig. 3. Logarithmic plots of the reverse characteristics of Au/β SiC contact diodes. (1): 4° off-axis (100) Si (NCSU870715). (2): 2° off-axis (100) Si (NASA 721/6) (3): Nominal (100) Si (NASA 816/2). (4): 4° off-axis (100) Si (NCSU 870626/1).

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